SynaptiCAD and Actel Upgrade Libero IDE with Reactive Test Bench Generation

SynaptiCAD, an EDA company specializing in timing diagram editing and test bench generation, announces a product partnership with Actel, a supplier of innovative programmable logic solutions.

"This product alliance expands the already abundant FPGA design capabilities of Actel's Libero Integrated Design Environment (IDE) development suite to include reactive test bench generation and VCD file reading and editing," said Saloni Howard-Sarin, director of antifuse products and tools marketing at Actel.

"The Reactive Test Bench Generation allows users to describe single timing diagram test benches that react to the user's HDL design files and generate pass/fail reports. This feature dramatically simplifies the analysis of the simulation results," according to Donna Mitchell, vice president of marketing at SynaptiCAD.

Reactive Simulation Checks

With "Reactive Test Bench Generation," users have the option of drawing "expected" waveforms on the Model Under Test output ports and adding "samples" to the waveforms to test for specific cases. During simulation, the code generated by the samples watches the output from the model under test and compares it to drawn states. The samples can perform a variety of functions such as pausing the simulation to debug a problem, reporting errors and warnings, user-defined
actions, and triggering other samples.

Reactive Loops Conditional Apply Stimulus

Users place markers in their timing diagram to wait for activity from the model under test and/or loop over a section of the diagram. Markers can also be used to call user-written HDL functions and tasks from within a diagram.

Clocked and Time-Based Test Bench Generation

Reactive test bench generation also allows the option of creating "clock-based" test benches as well as the "time-based" test benches currently supported by the stimulus-based generation models. Clock-based test benches delay in clock cycles instead of being time based, allowing the user to change his clock frequency without needing to change his timing diagram. Clock-based test benches are also required when testing using high-speed cycle-based simulators.

VCD File Support

VCD files are stimulus files that are produced by Verilog simulators. The new Libero IDE Platinum can read in VCD waveforms from previous simulations and use this data as the starting point for a reactive test bench.

Existing Support

SynaptiCAD and Actel have been working together since 2001 to provide test bench generation for Libero IDE using SynaptiCAD's WaveFormer Lite software. WaveFormer Lite is currently shipped with all versions of the Libero IDE and generates simple stimulus-based test benches. Libero users also have the option of upgrading WaveFormer Lite to WaveFormer Pro to gain access to SynaptiCAD's interpreted simulation engine, timing analysis, and test equipment support.