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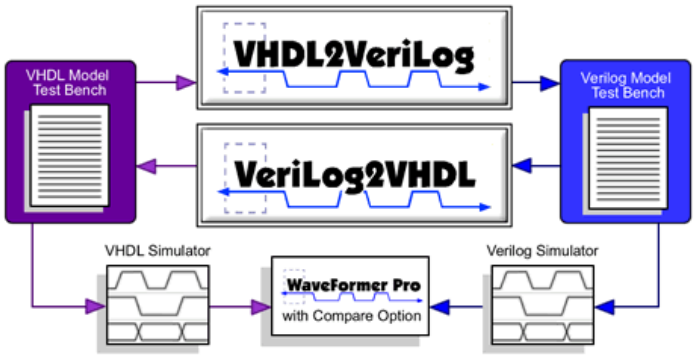
V2V
Verilog-to-VHDL und VHDL-to-Verilog Converter

VHDL2VeriLog oder VeriLog2VHDL



Neu in Version 17:

V2V - Verilog-to-VHDL model translation

- Support for Verilog-2005 multidimensional array translation.
- Added support for translating Verilog-2005 **signed rets** and **nets** into VHDL **numeric_std.signed** data types.
- Allow continuous assignments with undeclared targets to generate correct variable declarations for the targets.
- Support Verilog-2005 event control expressions such as **@(posedge foo, posedge bar)** as a synonym for **@(posedge foo or posedge bar)**.
- Support for Verilog-2005 **localparam** keyword.
- Support Verilog-2005 module parameter port lists.
- Support Verilog-2005 named parameter assignments.

V2V = VHDL-to-Verilog model translation

- Adds range to parameters generated from constants in vhdl2verilog when possible.
- Added **-Convert_Integers_for_Synth** option which translates vhdl integer literals into fixed-length bit strings.