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EDV BERATUNGS- UND HANDELSGESELLSCHAFT
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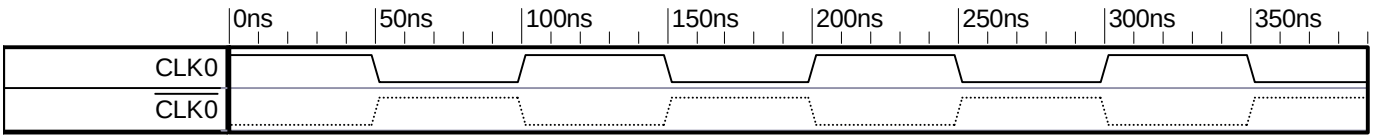
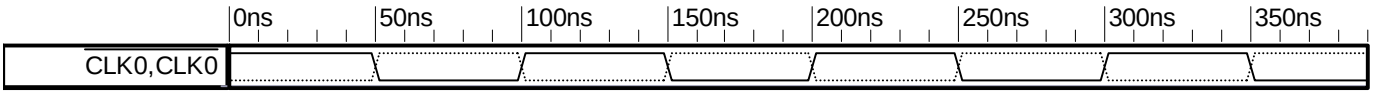
New Features for Version 10.04a

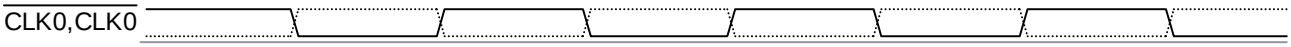
Timing Diagrammer Pro - All SynaptiCAD Products:



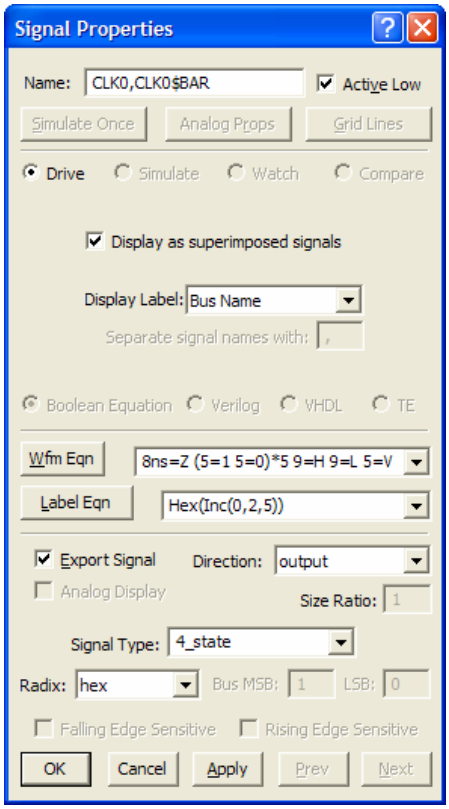
Since SynaptiCAD Product Suite 10.04a there is a great way of displaying true/complement signals in one line – dies sind die Worte eines deutschen Kunden.



oder so:



- Ability to superimpose signals to represent "differential" signals for **Group Buses**
  - Select the **Display as superimposed signals** checkbox in the Signal Properties dialog



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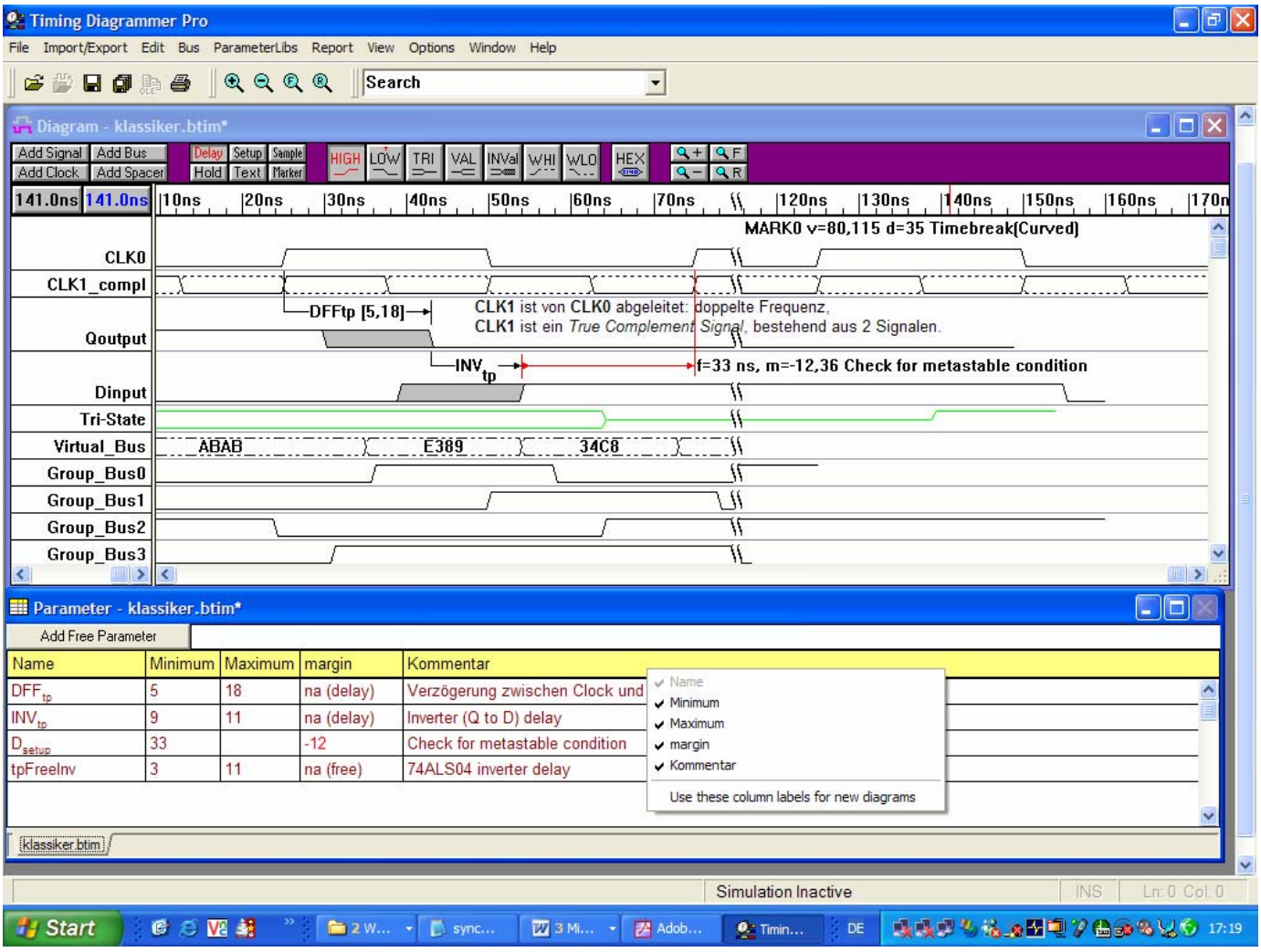
Change column titles for parameter table

Double-click column name in Parameter Window to edit name

Name	Minimum	Maximum	margin	Kommentar
DFF_{tp}	5	18	na (delay)	Verzögerung zwischen Clock und Ausgang Q
INV_{tp}	9	11	na (delay)	Inverter (Q to D) delay
D_{setup}	33		-12	Check for metastable condition
tpFreeInv	3	11	na (free)	74ALS04 inverter delay

Set which columns are printed in Parameter Table

Right Click column headers in Parameter Window to select columns



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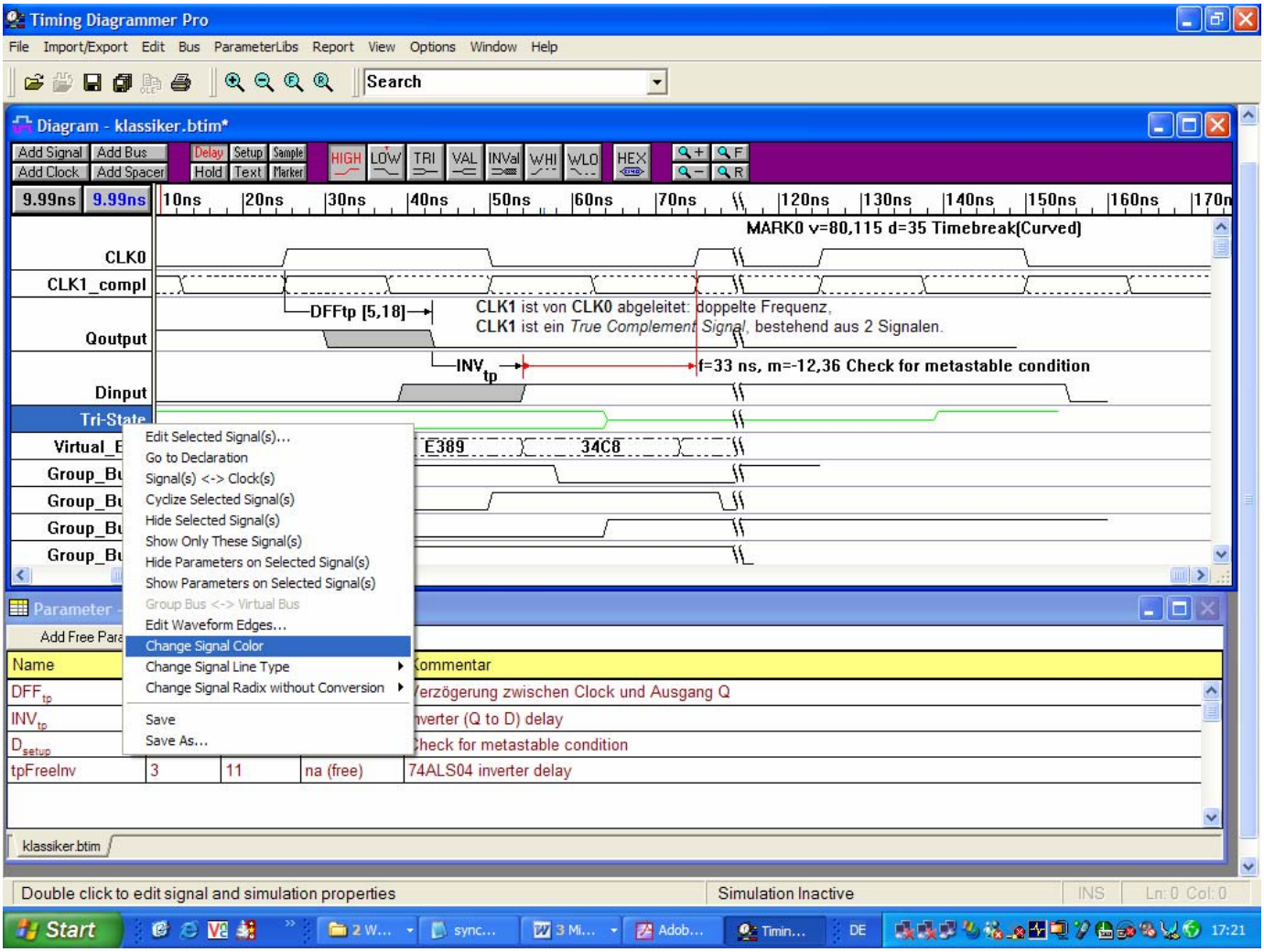
Set color of individual signal waveforms

Right click signal name in Diagram Window and select the Change Signal Color menu option



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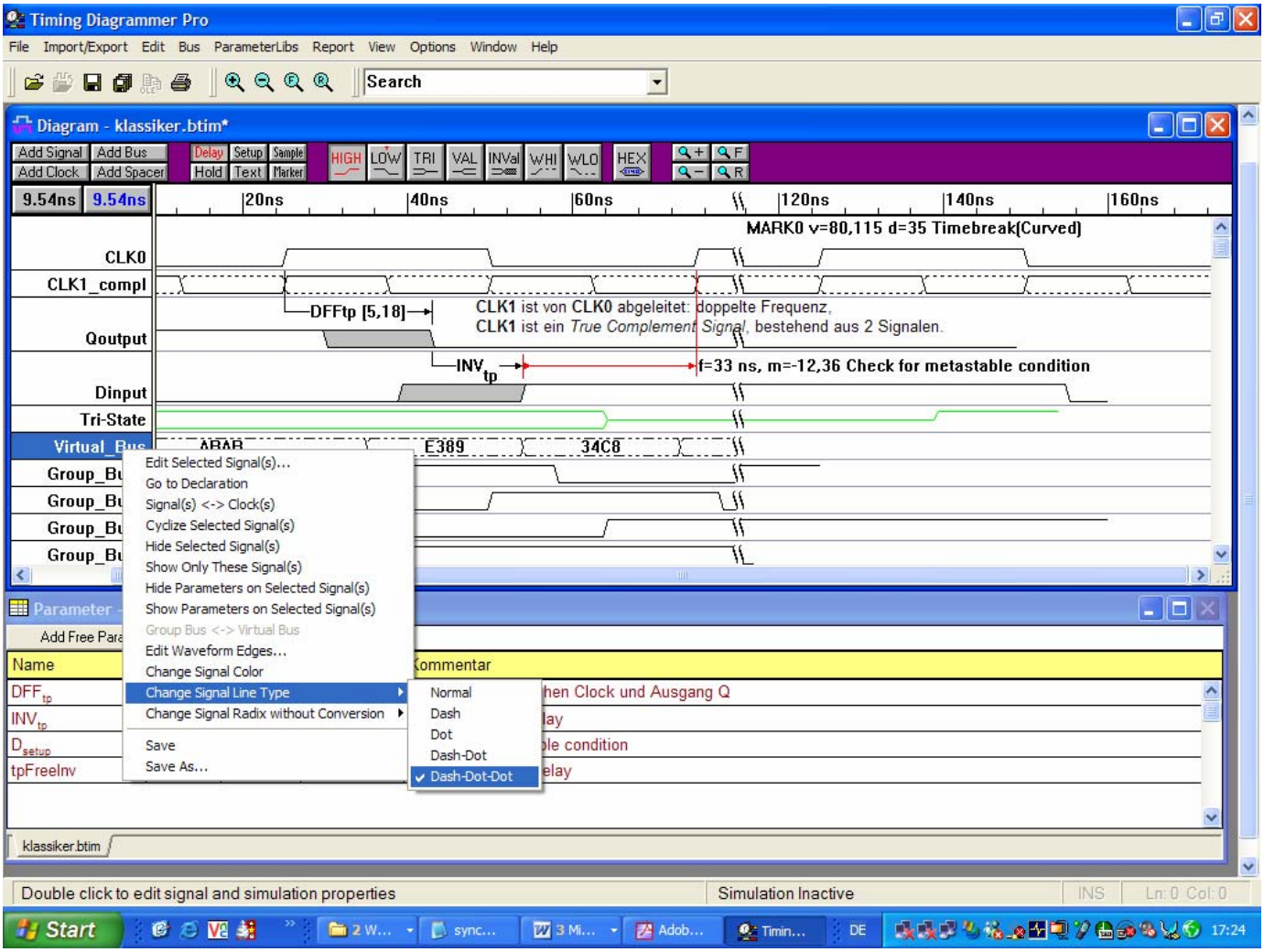
Set line style of individual signal waveforms (e.g. dotted, dashed, etc)

Right click signal name in Diagram Window and select the **Change Signal Line Type...** menu option



- Option to place white boxes under text so that text is never overwritten by other graphics in the diagram when images are created
    - De-select the **Transparent Text Object Background** option in the Drawing Preferences dialog
- Ability to specify width of EPS images (especially ability to create larger than A size paper images)
- Use Specify Image Size and specify the Width and Height in the Print dialog.
- Horizontal Justification for Text Objects
- Select Left, Center or Right justification in the Edit Text dialog.
- Speed up Expanding bus signals into individual bits.
- Sped up drawing grids in diagrams with a large numbers of signals.
- Expanded CORBA API that allows third party software to control the SynaptiCAD tools.
- Support for USB dongles (for newer laptop users which don't have parallel port)
- Faster startup on Linux, Solaris, and HPUX platforms
- CUPS printing support on Unix platforms (in addition to printcaps)
- Many bug fixes and various performance enhancements.

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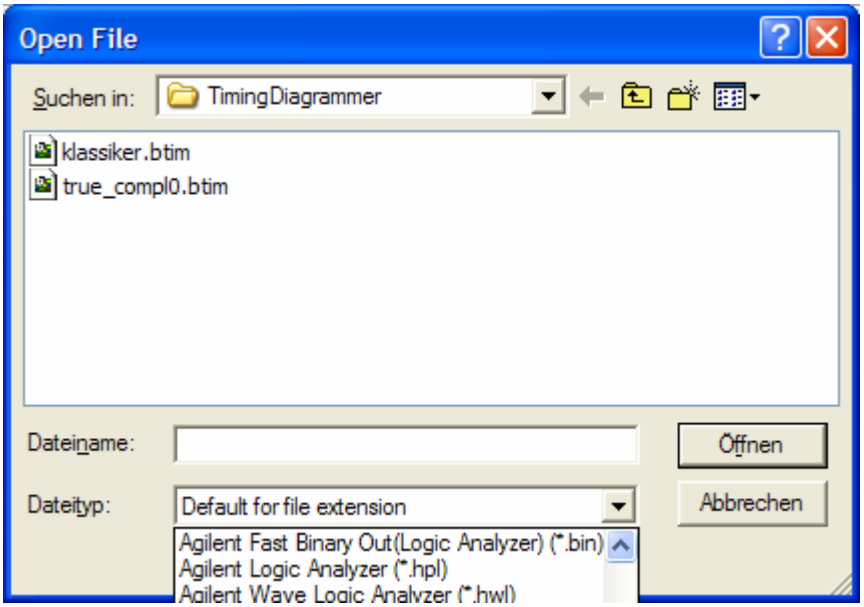
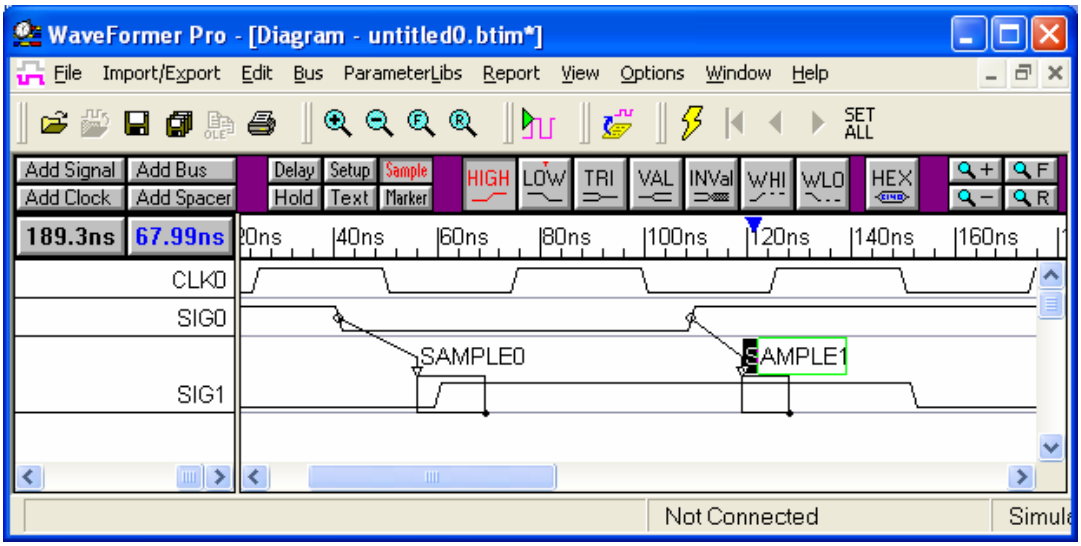
WaveFormer Pro

- Support for reading **Agilent 16900 Logic Analizer** ASCII data capture (.csv)



- **Tutorial on Reactive TestBench Generation** features. This tutorial introduces some of the optional reactive test bench feature set, which is included with TestBencher Pro and can be optionally added to Waveformer Lite, Waveformer Pro, Datasheet Pro, and BugHunter Pro. The tutorial covers creating cycle-based test benches, for-loop markers, bi-directional signals, waiting on events driven by the model under test (MUT), and verifying the output the MUT.



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TestBencher Pro

- Added **Delay After Clock Edge** option to Diagram Settings which contains two options: **Fixed** and **As Drawn**. If "Fixed" is selected, the user can specify the fixed amount of the delay. This affects code generated for clocked signals. The default behavior is Fixed 0. This replaces the Include Time Delays option in previous versions of TestBencher Pro. Previous projects will be converted as follows:

  Include Time Delays ON => As Drawn

  Include Time Delays OFF => Fixed 0

- All **Note** and **Warning** messages output by TestBencher Pro during simulation can now be enabled/disabled via two variables, EnableNoteMessages and EnableWarningMessages. These messages can also be enabled/disabled at compile time for Verilog projects, by defining TB_DISABLE_NOTE_MESSAGES and/or TB_DISABLE_WARNING_MESSAGES.
- Enhanced messages generated for **Sample Display Message** action. These messages were made more intuitive based on the level of severity and what exactly is drawn in the diagram.
- **Add timestamp to each file checkbox** added to Project Generation Properties. This is useful if the generated code is versioned and you don't want the generated file to be different just because the time is different.
- **Prefix Generated Files With** edit box added to Project Generation Properties. This can also be useful if the generated code is versioned where you may want to provide keywords to the versioning system.
- **Indent Size** added to Project Generation Properties. Affects all generated code in the project.
- Added tool tip to display current and top scopes for toolbar "S" and "s" buttons.
- Added **Display Applied Inputs** verbose option to Diagram Settings.
- New **Pipeline Boundary** marker type which makes the construction of pipelined transactors much easier and automatic.
- Added PDF documents to explain following TestBencher Pro examples in detail: AMBA, PCI, pipelining, uarttest, VME. These can all be found in the <SynaptiCAD Installation Directory>\install\Examples\docs directory.
- Added **Initial Value** field for project and diagram variables.
- Added extended comment block at top of generated transactors that summarizes the contents of the transactor.
- **Sim Diagram** (not Sim Diagram and Project) will now drive Input signals. This allows you to test out simulated signals contained in a transactor before integrating it into the project.
- Added **syncad_vhdl_lib** and **syncad_verilog_lib** which contains a collection of base modules that the Testbencher Pro generated code uses. This library needs to be compiled once per installation of TestBencher Pro and is done via the **Compile Syncad Libraries** button in the **Options > Simulator/Compile Settings** dialog. Use of these libraries helps speed up the compilation time of individual projects.

- Added new clock models for use in VHDL which are used to more accurately simulate the clocks drawn in TestBencher Pro's transactor diagrams. These are a part of the new **syncad_vhdl_lib**.
- Cosmetic cleanup to **Class Method** generation.
- **For Loop Markers** in VHDL are now implemented using while loops so that the loop index can be declared as a shared variable and accessed anywhere in the diagram.
- Added two new folders under each transaction diagram in the project window: **Included External to Module** and **Included Internal to Module**. These folders allow easy access to user included files and is linked to the Diagram Properties dialog.
- Added support for multiple diagram instances in VHDL.
- Added **FIFO Semaphore** feature. **Semaphores** are created in the Project's **Class Library and Variables** dialog.